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DMD-based autostereoscopic display system for 3D interaction

Ying Zhang and Adrian R L Travis
Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue,
Cambridge CB3 0FA, UK
{yz282; arlt1@cam.ac.uk}

A novel approach to implement the multiview autostereoscopic display system is presented. This implementation brings together a high frame rate digital micro-mirror device (DMD) projector, an active shutter, and an optical wedge. It facilitates the modulation of the DMD to achieve extra high frame rate with a trade-off in greyscale resolution. The results have the great potential for commercialising the autostereoscopic display system.

Introduction: Autostereoscopic display systems provide the viewers with 3D perception of images without the need of wearing either a pair of special glasses or other headsets. Two common approaches are available to realise an autostereoscopic display system: spatial-multiplexing and time-multiplexing [1 - 4]. Cambridge University has been developing an autostereoscopic display system by using the time-multiplexing approach for about 20 years, and has achieved great success [3 - 5]. However, owing to the lack of a high bandwidth display device, Cambridge's previous system adopted the view-sequential approach to encode depth information, and used fast cathode ray tubes (CRTs) to generate pixel information. On the basis of the success of Cambridge's 3D display system, and the fast advancement of spatial light modulator (SLM) technology, especially DMD technology [6], over the years, this Letter introduces our innovation of the existing system by using DMDs and a decoupling diffuser to replace the CRTs. It is well known that the high pixel bandwidth is of critical importance to a 3D display system, since it almost requires orders of magnitude more information than its 2D counterpart [1, 2]. A CRT is an analogue device, bulky and difficult to run; while a DMD is a binary device with the features of high speed, high precision and broadband capacity, allowing for encoding the desirable quantity of 3D information and realising the time-multiplexing system much easier [7].

Principle and system components: This system uses a time-multiplexing approach. It consists of three major parts (see Fig. 1): a high frame rate DMD projector, an active shutter, and an optical wedge [8]. Three DMDs are utilised, one for each colour: red, green, and blue (RGB). An optical wedge is brought in, making the whole display system in a flat panel form. The following sections firstly describe the

high frame rate projector, the DMD, the shutter, and the optical wedge, respectively, and then describe the overall implementation. Finally, the conclusions are given.

High frame rate projector: Since the projector is a high-bandwidth image source in this system, it must be able to generate sufficient images to support the creation of the 3D perspectives. The maximum number of views of the 3D perspectives in an autostereoscopic display system equals the frame rate divided by the temporal bandwidth of the human eye. This system uses a self-built projector, which is centred on three Texas Instruments (TI) Corp's DMDs, one for each RGB colour. It can render 1500 images/s where each image is 1024×768 pixels with 24 bit RGB (8 bits per colour). Hence, if the temporal bandwidth of the human eye is assumed to be approximately 50Hz, the projector can support 30 views of 3D perspectives. The computed 3D perspectives are fed into the projector's onboard frame buffer from a PC. The frame buffer is double buffered allowing one frame of image to be loaded while another is displayed. From the frame buffer the images are fed into the formatter, which in turn sends the correct bit sequence to each DMD. Each time, while a new image is read from the frame buffer, a pulse is sent to the shutter controller which controls the shutter (see Fig. 1). The controller has an onboard counter which cycles through each slit.

DMD: The merits of the DMD make it a very attractive device for miniaturising Cambridge's 3D display system. A DMD consists of many moving micro-mirrors that are controlled by underlying CMOS electronics. The mirrors are highly reflective for modulating light, thus making the DMD an optical MEMS as well as a reflective SLM. A superstructure array of micromechanical mirrors is functionally located over memory cells of the SRAM inside a DMD. A memory cell, which is loaded with a logical '1', positions the mirror, through electrostatic forces, reflecting the incident light into the aperture of the projection lens. A memory cell, which is loaded with a logical '0', positions the mirror directing away the incident light from the projection lens and into a light sink. All the 'on' state light is optically recombined with the other colour components and projected onto the viewing screen. This research uses a 0.7 XGA LVDS DMD for each RGB colour. It has 1024×768 micro-mirrors in the array, supporting the data transmission rate up to 12.8 Gbits/s. This is sufficient for the delivery of 1500 frames/s at a greyscale resolution of 8 bit per RGB colour, which requires the data transmission rate to be at least $1500 \times 8 \times 1024 \times 768 \approx 9.44$ Gbits/s.

Shutter: The shutter completes the time-multiplexing mechanism, and locates between the DMD projector and the wedge (see Fig. 1) in the current setup. It consists of many narrow slits that can switch between optically opaque and transparent at a specified high speed. This system uses a ferroelectric liquid crystal (FLC) shutter taken from Cambridge's previous system. The shutter was manufactured by a company called Crlopto.com. Its switching speed is about 50 μ s, sufficiently fast for the frame rate of 1500 frames/s. The contrast is about 80:1. Currently, the ideal position of the shutter is under investigation.

Optical wedge: The wedge is a simple optical waveguide, which is made of optically transparent materials, and works through internal reflection [8]. A ray, which is injected into the wedge, bounces up within the waveguide until it reaches the critical angle, at which point it exits the wedge. By ensuring that the rays focus on the exit plane, a flat panel display can be created by inserting a diffuser at the exit plane. The diffuser is required, since the rays exit the waveguide almost vertically. In this system, the image from the DMD projector is injected into the wedge (see Fig. 1). The size of the image seen on the diffusive exit-surface purely depends on the size and the design of the wedge. Therefore, the screen size can be purely adjusted by changing the wedge optics.

System implementation: The major parts of this system are implemented by using TI's DMD Discovery 3000 development platform; its core part is a DDC3000 controller. The DDC3000 chipset consists of a SNDDISCO3000 configurable flash PROM, a Xilinx Spartan-3 FPGA, a DAD1000 power and reset driver, and a DMD. The hardware concept and dataflow of the implementation is shown in Fig. 2a. The DMD data access is organised in sequences of FPGA frames. Each sequence is a series of images to be displayed, all images in a sequence have the same bit-depth, and the different sequences may be defined and loaded at the same time. The SDRAM onboard memory stores the XGA image sequences, which are pre-loaded for subsequent high-speed display. USB 2.0/DVI interfaces realise the PC connection for data transmission. The maximum onboard storage capacity is 1 Gbit, which is not mapped to the PC.

The heart of the application hardware is a Xilinx Virtex-4 FPGA (i.e. APPSFPGA), which links the onboard image sequence memory (i.e. SDRAM) with the DMD (via DDC3000). The FPGA logic design includes all the timing and control facilities necessary to load and to switch the DMD according to the user-defined properties of the sequence selected for display. The FPGA is also programmed to

realise the pulse width modulation display of greyscale images with flexible bit-depth. Both sequence pre-loading from PC to SDRAM and sequence displaying from SDRAM to DMD are implemented to run in parallel for two different sequences, that is, a new image sequence is loaded while another image sequence is displaying. V-Syn and Z-Syn yield precise synchronisation between the DMD operation and the shutter. The APPSFPGA is programmed to run as a master to generate the corresponding synchronisation signals for the shutter and LED light source at image level within the sequence. A module for accessing and controlling the onboard memory, which uses DDR2 SDRAM, also has been implemented within APPSFPGA, enabling the data can be transferred on both edges of the clock cycle. The block diagram of the system hardware is shown in Fig. 2b.

The corresponding software (see Fig. 3) is based on Microsoft Visual Studio development environment, running under Microsoft Windows XP OS. In general terms, the desired high-speed DMD operations are coded as a binary pattern (bit-plane image) sequence with the addition of certain timing parameters. The pattern can be generated by the user program or loaded from the hard disc of the PC, and the sequences are then pre-loaded to the onboard memory. The display process can be finally initiated by application software. A 3D library, which encapsulates all functionalities for controlling the data loading and the high-speed display of the binary pattern sequences, is developed. Various applications can be implemented on the base of this function library. It communicates with the USB 2.0/DVI interface drivers to transfer image sequence data into the onboard memory. Finally, the FPGA logic controls the communication with the DDC3000 chipset, thus controlling the DMD mirrors. All layers below the library are transparent to the application programs so that DMD programming is significantly simplified, thus accelerating the applications development.

Conclusions: A multiview autostereoscopic display system is initially setup. It produces 30 distinct perspectives with about 14° viewing angle and roughly 30 cm visual zone. Its advantage is that the viewer can perceive a 3D image without the positional constraints of both eyes in the viewing zones. It can accommodate multiple viewers, with each viewer seeing a corresponding 3D image. Looking around objects in the scene simply requires the viewer moving head, while head-tracking is not required. Its weakness includes the complexity of generating all the views simultaneously, since each view is always being displayed, whether a view is seen by a viewer or not. Specially, it needs a

particular approach to generate and deliver the data at an ultra-high frame rate to meet the demand of time-multiplexing, synchronising with the sequential on-off switch of the FLC shutter. Future work includes overcoming the image distortions in the optical wedge, increasing the number of views, and optimising the shutter position in the path of light modulation.

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Figure captions:

Fig. 1 Block diagram of the projection system

Fig. 2 (a) Hardware concept and dataflow of the system; and (b) block diagram of the system hardware

Fig. 3 Software architecture and layers

Figure 1

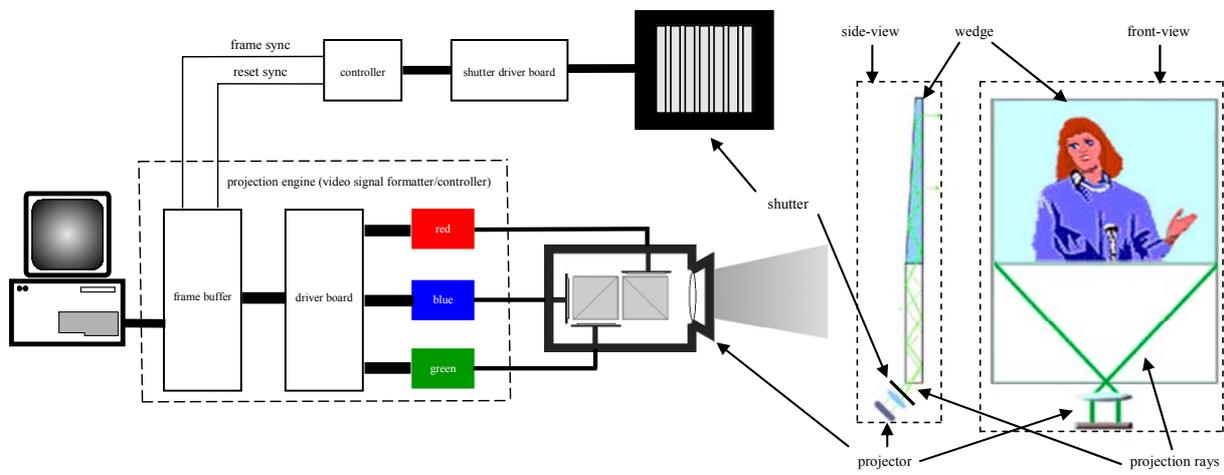
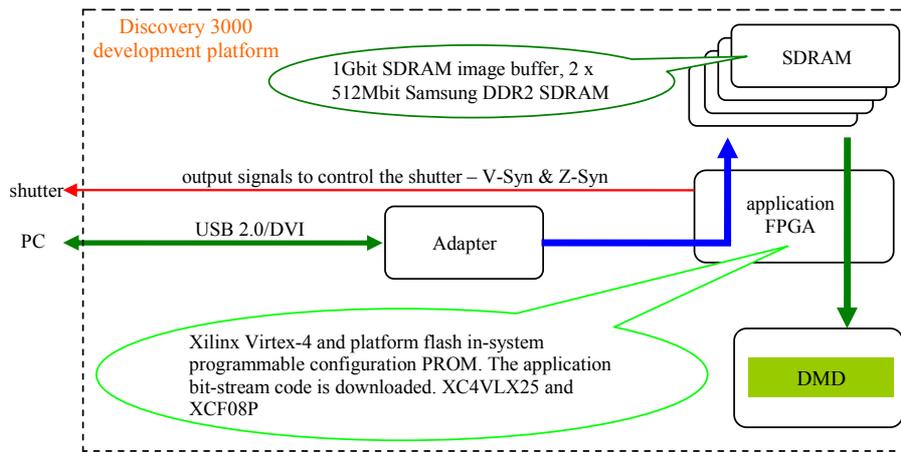
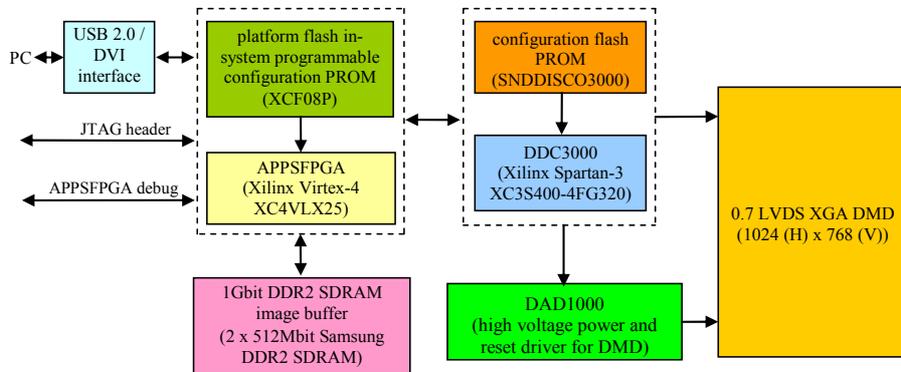


Figure 2



(a)



(b)

Figure 3

